



Attorney's Docket No.: 10559-601001/P12885

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

01-05-04

Applicant : William R. Wheeler et al.
Serial No.: 09/942,116
Filed : August 29, 2001
Assignee : Intel Corporation
Title : LOGIC SIMULATION

Art Unit: 2185
Examiner:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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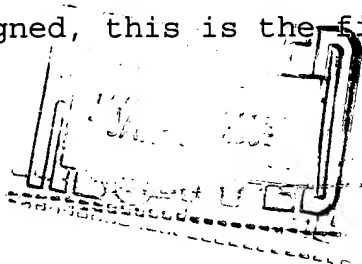
INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first Office action on the merits. No fee is required.

Each enclosed document listed on the herewith Form PTO-1449 was cited in the attached International Search Report dated December 5, 2003, issued in a foreign counterpart application not more than three months ago. To the best knowledge of the undersigned, this is the first citation of these items in any



CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 23, 2003

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Jennifer H. Payne

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communication from a foreign patent office in a counterpart
foreign application.

The documents are in the English language; hence no concise
explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the
return of a copy of the enclosed form PTO-1449 with the
Examiner's initials in the left column per MPEP 609 are
earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit
Account No. 06-1050.

Respectfully submitted,

Date: 12/20/03



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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-601001	Application No. 09/942,116
Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant William R. Wheeler et al.	
		Filing Date August 29, 2001	Group Art Unit 2185

(37 CFR §1.98(b))

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	5,603,015	02/1997	Kurosawa, et al.			
	AB	5,604,894	02/1997	Pickens, et al.			
	AC	5,694,579	12/1997	Razdan, et al.			
	AD	5,706,476	01/1998	Giramma			
	AE						
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	AG						
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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL	0 404 482	12/1990	EPO				
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	Parlakbilek, et al., "A Multiple-Strength Multiple-Delay Compiled-Code Logic Simulator", <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 12(12):1937-1946 (1993).
	AR	
	AS	
	AT	

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	